IEEE Signal Processing Magazine
Special Issue on Signal Processing on Platforms with Multiple Cores: Part 2 -- Design and Applications

Multi-core processors are now prevalent everywhere from desktops and graphics processors to laptops and embedded systems. It is clear that signal processing systems of tomorrow will be (and must be) implemented on platforms with multiple cores. Signal processing algorithm designers must understand the nuances of a multi-core computing engine, only then can the tremendous computing power that such platforms provide be harnessed efficiently.

This special issue is a follow-up of an earlier special issue on general trends, overview and design methodologies for signal processing on systems with multiple cores that will appear in the Nov. 2009 issue of the IEEE Signal Processing magazine. The intention of this special issue is to attract tutorial-style papers on (1) novel applications that can be enabled by platform with multiple cores, and (2) design examples of signal processing on platforms with multiple cores that demonstrate the techniques or algorithm changes for efficient implementations. Possible topical areas include, but are not limited to, the following topics.

Scope of topics:

1. Audio, speech and language processing
2. Image, video and multimedia signal processing
3. Biomedical signal processing and bioinformatics
4. Wireless communications and networking
5. Sensing and sensor signal processing
6. Machine language for signal processing
7. Information forensics, security and cryptography

If possible, please make sure the work is applicable to a broad scope, e.g., (1) optimized implementations on multiple multi-core platforms, (2) implementation of multiple algorithms, or (3) scalable implementations that are applicable to more than tens or even hundreds of cores.

Submission Procedure:

Before writing full manuscripts, prospective authors are asked to submit proposal-like white papers to the web submission system at http://www.ee.columbia.edu/spm/ according to the following timetable. The white paper should summarize the key takeaway messages ("What can the reader learn from the paper?"), the motivation ("Why should a reader read the paper?"), the significance of the topic ("Why is this topic important?"), a brief history ("What are the related work and authors' prior publications in this topic?"), and the outline of the content ("What do you plan to write in the full manuscript?"). The authors should properly answer all the questions above so that the white paper can be reviewed efficiently. After answering the above questions, the authors can selectively describe some details within the rest of page limit. Please be aware that the importance of multi-core platforms will be addressed in depth in the November special issue. Please keep this in mind and avoid dwelling on the general motivation and importance of multi-core platforms, as such content will be redundant with the November issue. The white paper should be no more than 2 pages in the IEEE single-space double-column format.

Schedule:

- White paper due: March 1, 2009
- Decision based on the white paper: May 1, 2009
- Initial full paper due: July 15, 2009
- Decision based on the initial full paper: August 31, 2009
- Revised full paper due: Sept 30, 2009
- Review complete for the revised manuscript: Oct 31, 2009
- Final manuscript due: Nov 15, 2009
- Target publication date: March 2010

Guest Editors:

Yen-Kuang Chen	Chaitali Chakrabarti	Shuvra Bhattacharyya	Bruno Bougard
Intel Corporation	Arizona State Univ.	Univ. of Maryland at College Park	Septentrio N.V.
USA	USA	USA	Belgium
yen-kuang.chen@intel.com	chaitali@asu.edu	ssb@umd.edu	bruno.bougard@septentrio.com